General Description：

105N08 , the silicon N-channel Enhanced VDMOSFETs, is obtained by the high density Trench technology which reduce the conduction loss, improve switching performance and enhance the avalanche energy. This device is suitable for use as a load switch and PWM applications. The package form is TO-220AB, which accords with the RoHS standard.

Features：

- l **Fast Switching**
- l **Low ON Resistance(Rdson≤8.0mΩ)**
- l **Low Gate Charge**
- l **Low Reverse transfer capacitances**
- l **100% Single Pulse avalanche energy Test**

Applications：

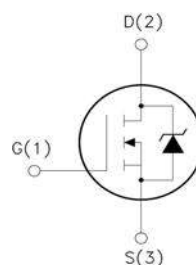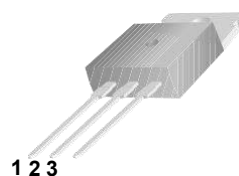Power switch circuit of adaptor and charger.

V_{DSS}	80	V
I_D（Silicon limited current）	105	A
I_D（Package limited）	60	A
P_D	138	W
$R_{DS(ON)Typ}$	6.2	mΩ

TO-220AB

1 2 3

1.Gate (G)
2.Drain (D)
3.Source (S)

Absolute（T_j= 25℃ unless otherwise specified）

Symbol	Parameter	Rating	Units
V_{DSS}	Drain-to-Source Voltage	80	V
I_D	Continuous Drain Current	105	A
	Continuous Drain Current T_C = 100 °C	66	A
I_{DM} a1	Pulsed Drain Current	420	A
V_{GS}	Gate-to-Source Voltage	±20	V
E_{AS} a2	Avalanche Energy	462	mJ
P_D	Power Dissipation T_C = 25 °C	138	W
	Derating Factor above 25°C	1.11	W/℃
T_J，T_{stg}	Operating Junction and Storage Temperature Range	150，−55 to 150	℃
T_L	MaximumTemperature for Soldering	300	℃

Electrical Characteristics（T_j= 25℃ unless otherwise specified）：

OFF Characteristics						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
V_{DSS}	Drain to Source Breakdown Voltage	V_{GS}=0V, I_D=250µA	80	--	--	V
I_{DSS}	Drain to Source Leakage Current	V_{DS}=80V, V_{GS}= 0V, T_j = 25℃	--	--	1	µA
		V_{DS} =64V, V_{GS}= 0V, T_j = 125℃	--	--	100	
$I_{GSS(F)}$	Gate to Source Forward Leakage	V_{GS}=20V	--	--	100	nA
$I_{GSS(R)}$	Gate to Source Reverse Leakage	V_{GS} =-20V	--	--	-100	nA

ON Characteristics						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
$R_{DS(ON)}$	Drain-to-Source On-Resistance	V_{GS}=10V,I_D=40A	--	6.2	8.0	mΩ
$V_{GS(TH)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250µA	2	3	4	V
Pulse width tp≤300µs, δ ≤2%						

Dynamic Characteristics						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
R_g	Gate resistance	V_{GS}=0V, V_{DS}=0V, f=1MHz	--	1	--	Ω
C_{iss}	Input Capacitance	V_{GS} = 0V V_{DS} =40V f = 1.0MHz	--	3255	--	pF
C_{oss}	Output Capacitance		--	354	--	
C_{rss}	Reverse Transfer Capacitance		--	260	--	

Resistive Switching Characteristics						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
$t_{d(ON)}$	Turn-on Delay Time	V_{GS}=10V, R_G=6Ω V_{DD}=40V, I_D=40A	--	25	--	ns
tr	Rise Time		--	18	--	
$t_{d(OFF)}$	Turn-Off Delay Time		--	65	--	
t_f	Fall Time		--	23	--	
Q_g	Total Gate Charge	I_D =40A V_{DD} =40V V_{GS} = 10V	--	78	--	nC
Q_{gs}	Gate to Source Charge		--	14	--	
Q_{gd}	Gate to Drain ("Miller")Charge		--	33	--	

Source-Drain Diode Characteristics

Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
I_S	Continuous Source Current (Body Diode)	T_C = 25 °C	--	--	105	A
I_{SM}	Maximum Pulsed Current (Body Diode)		--	--	420	A
V_{SD}	Diode Forward Voltage	I_S=30A,V_{GS}=0V	--	--	1.2	V
trr	Reverse Recovery Time	di/dt=100A/us	--	36	--	ns
Qrr	Reverse Recovery Charge	IF=50A	--	52	--	nC
Pulse width tp≤300μs, δ ≤2%						

Symbol	Parameter	Max.	Units
$R_{\theta JC}$	Junction-to-Case	0.9	℃/W
$R_{\theta JA}$	Junction-to-Ambient	62.5	℃/W

[a1]：Repetitive rating; pulse width limited by maximum junction temperature
[a2]：L=0.5mH,Ias=43A   Start T_J=25℃

Characteristics Curve：
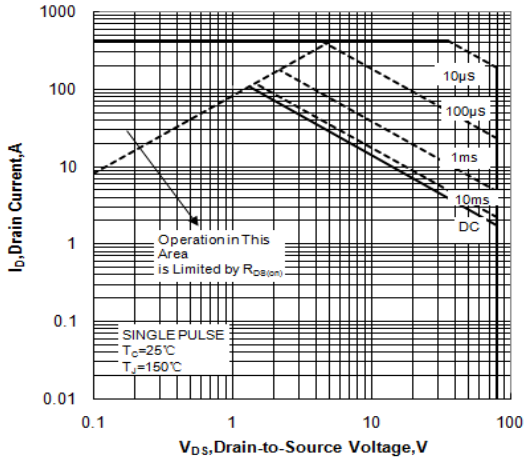
Figure 1.　Maximum Safe Operating Area
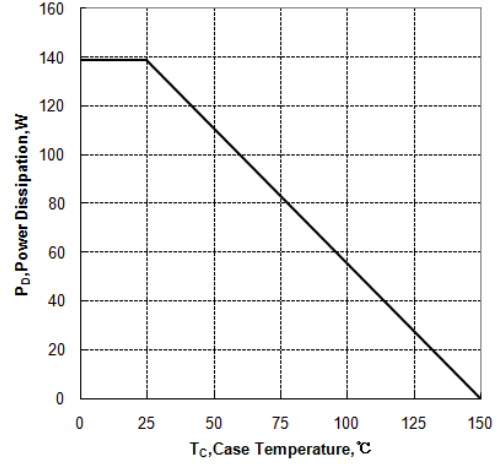
Figure 2.　Maximum Power Dissipation vs Case Temperature
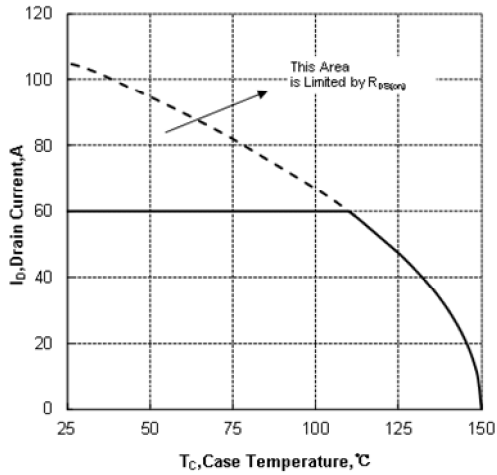
Figure 3.　Maximum Continuous Drain Current vs Case Temperature
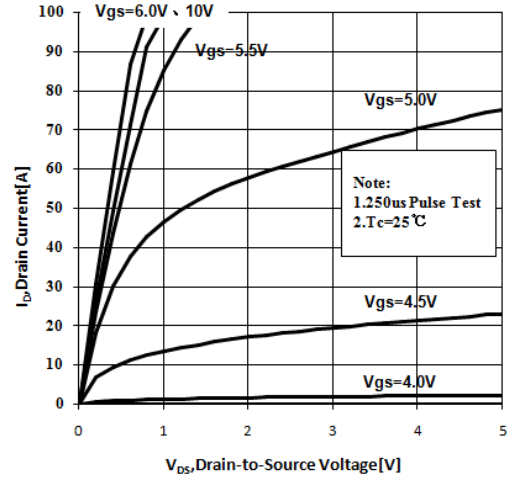
Figure 4. Typical output Characteristics
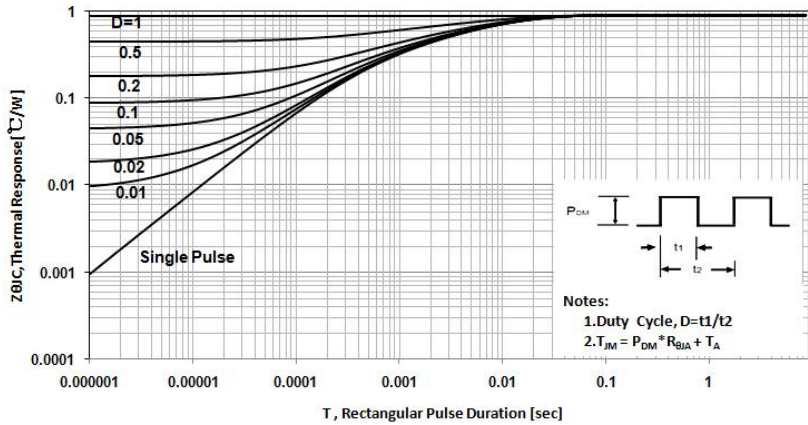
Figure　5　Maximum Effective Thermal Impedance , Junction to Case
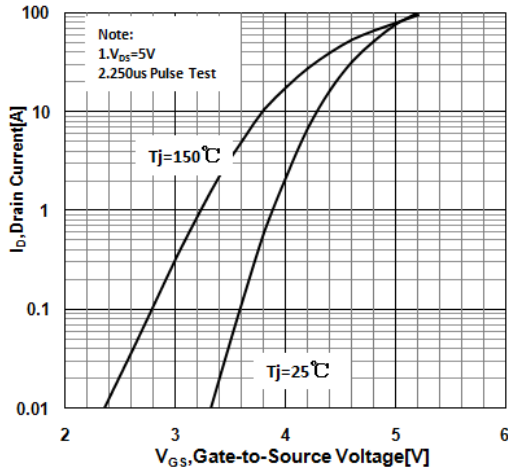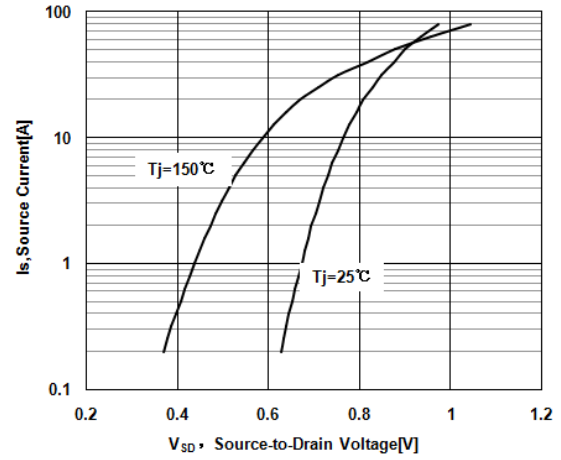
Figure 6 Typical Transfer Characteristics
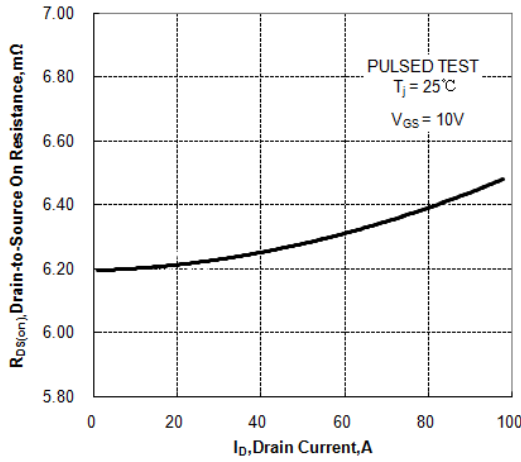

Figure 7 Typical Body Diode Transfer Characteristics
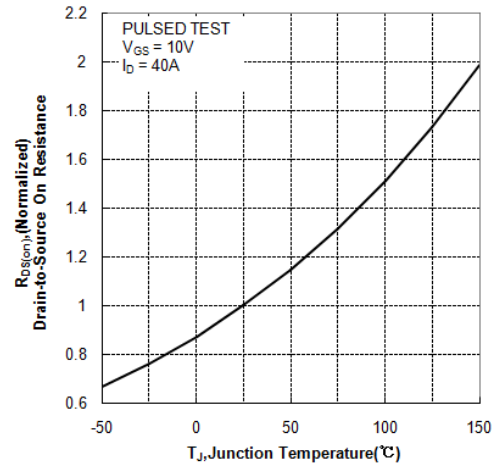

Figure 8. Drain-to-Source On Resistance vs Drain Current

Figure 9. Normalized On Resistance vs Junction Temperature
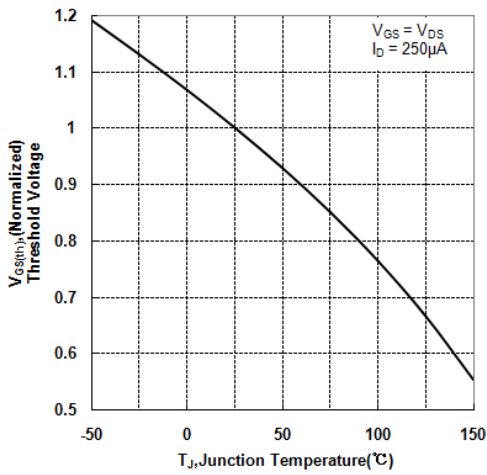
Figure10. Normalized Threshold Voltage vs

Junction Temperature
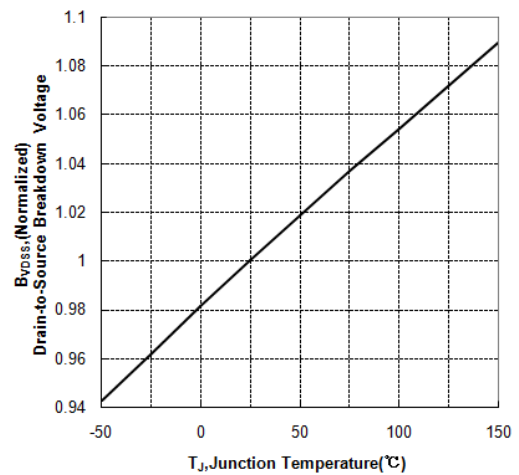
Figure 11. Normalized Breakdown Voltage vs

Junction Temperature
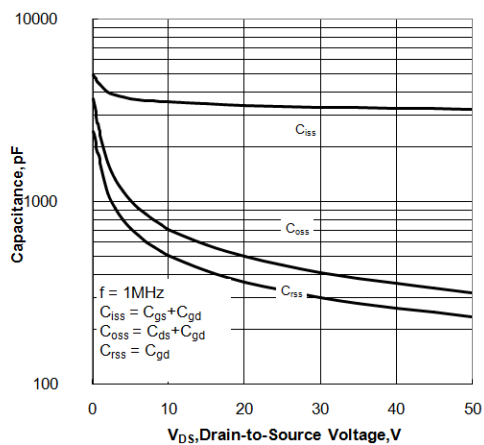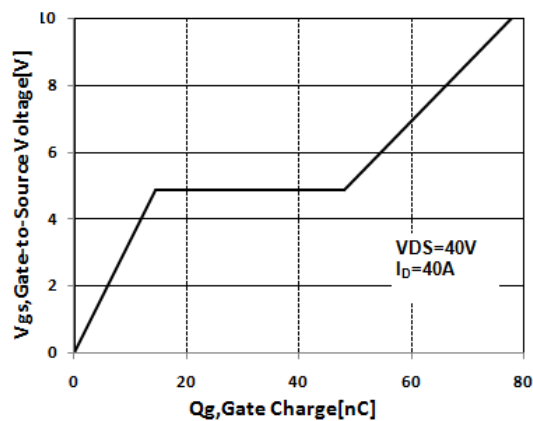
Figure 12. Capacitance Characteristics

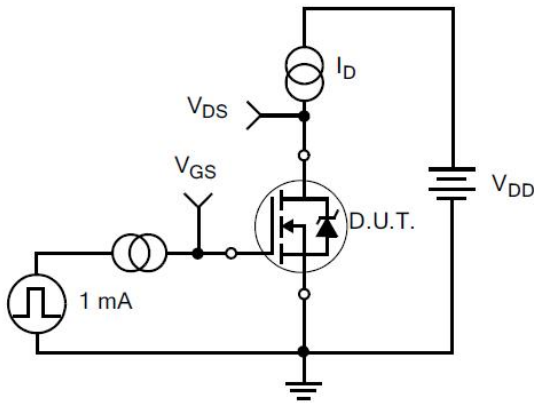Figure 13. Typical Gate Charge vs Gate to Source Voltage

Test Circuit and Waveform

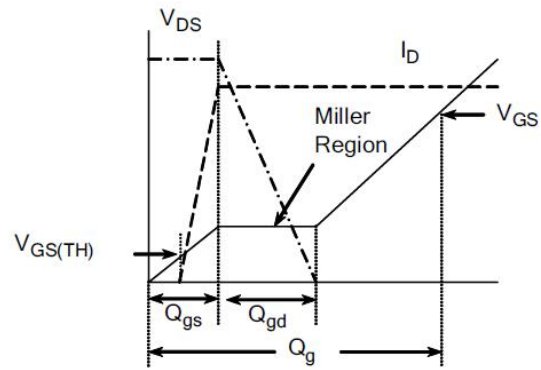Figure 14. Gate Charge Test Circuit

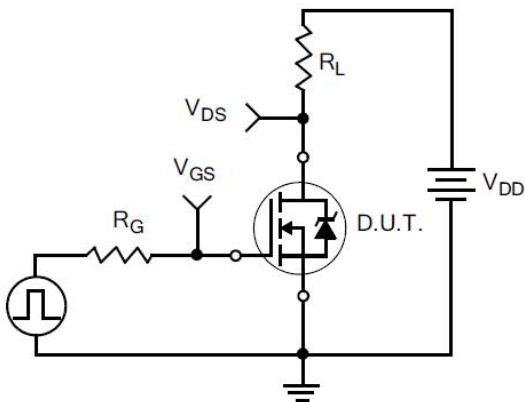Figure 15. Gate Charge Waveforms

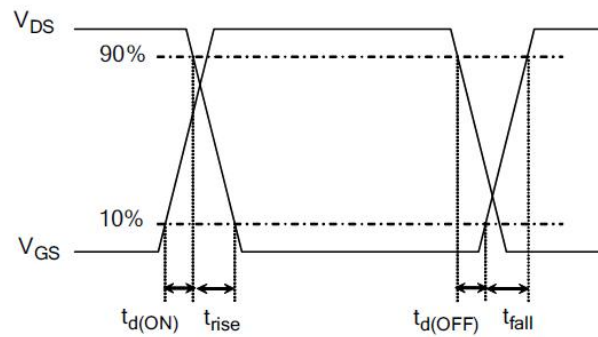

Figure 16. Resistive Switching Test Circuit

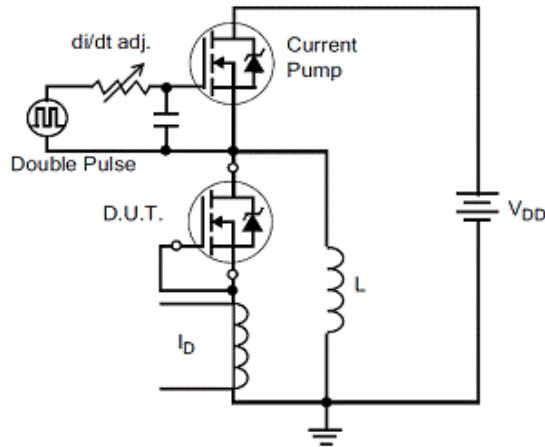Figure 17. Resistive Switching Waveforms

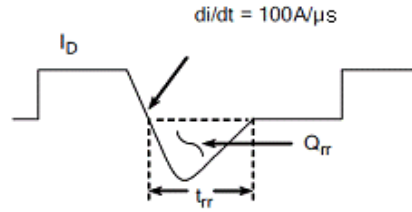**Figure 18. Diode Reverse Recovery Test Circuit**

Figure 19 .Diode Reverse Recovery Waveform

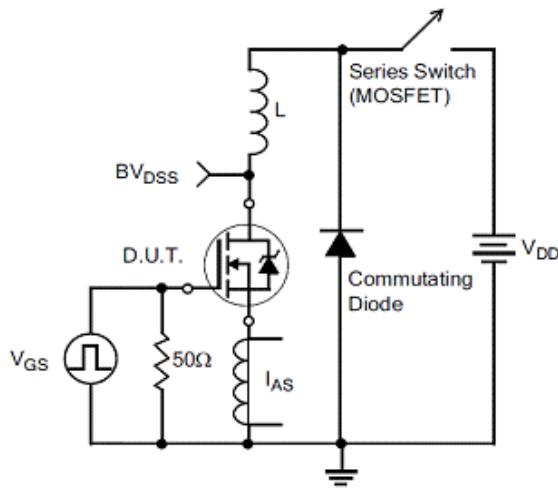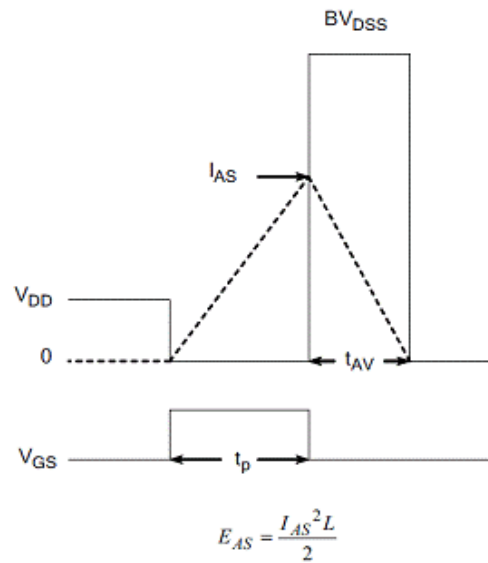**Figure20.Unclamped Inductive Switching Test Circuit**

$$E_{AS} = \frac{I_{AS}^2 L}{2}$$

Figure21.Unclamped Inductive Switching Waveform

Package Information：
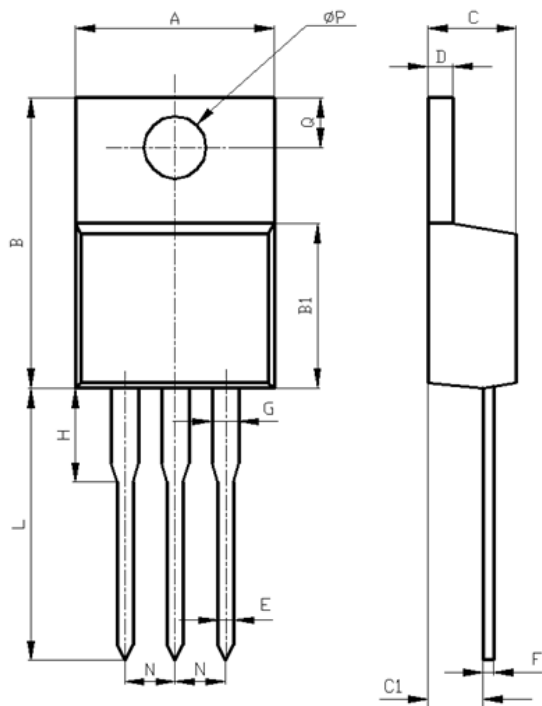
Items	Values(mm)	
	MIN	MAX
A	9.60	10.6
B	15.0	16.0
B1	8.90	9.50
C	4.30	4.80
C1	2.30	3.10
D	1.20	1.40
E	0.70	0.90
F	0.30	0.60
G	1.17	1.37
H	2.70	3.80
L*	12.6	14.8
N	2.34	2.74
Q	2.40	3.00
Φ P	3.50	3.90

*adjustable

TO-220AB Package